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JCS28 U.S. PTO1050 U.S. PTO  
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367910/01U.S. DEPARTMENT OF COMMERCE  
PATENT AND TRADEMARK OFFICEPATENT APPLICATION  
TRANSMITTAL LETTER  
UNDER 37 C.F.R. 1.53(b)ATTORNEY DOCKET NO.:  
2207/12116Assistant Commissioner  
for Patents  
Washington D.C. 20231  
Box Patent Application

Transmitted herewith for filing is a patent application.

Inventor(s): **Raj NAIR, Johanna SWAN, Bala NATARAJAN, and MARK BOHR**For: **SILICON INTERPOSER-BASED HYBRID VOLTAGE  
REGULATOR SYSTEM FOR VLSI DEVICES**

Enclosed are:

1. 7 sheet(s) of specification, 4 sheet(s) of claims, and 1 sheet of abstract.
2. 4 sheet(s) of drawings.
3. An Information Disclosure Statement along with an accompanying PTO-1449 form.
4. The filing fee has been calculated as shown below:

	NUMBER FILED	NUMBER EXTRA*	RATE (\$)	FEE (\$)
BASIC FEE				740.00
TOTAL CLAIMS	20 - 20 =	0	18.00	0.00
INDEPENDENT CLAIMS	4 - 3 =	1	84.00	84.00
MULTIPLE DEPENDENT CLAIM PRESENT			280.00	0
*Number extra must be zero or larger		TOTAL		824.00
If the applicant is a small entity under 37 C.F.R. §§ 1.9 and 1.27, then divide total fee by 2, and enter amount here.			SMALL ENTITY TOTAL	

5. Please charge the required application filing fee of **\$824.00** to the deposit account of **Kenyon & Kenyon**, deposit account number **11-0600**.

5. The Commissioner is hereby authorized to charge payment of the following fees, associated with this communication or arising during the pendency of this application, or to credit any overpayment, to the deposit account of **Kenyon & Kenyon**, deposit account number **11-0600**:

- A. Any additional filing fees required under 37 C.F.R. § 1.16;
- B. Any additional patent application processing fees under 37 C.F.R. § 1.17;
- C. Any additional document supply fees under 37 C.F.R. § 1.19;
- D. Any additional post-patent processing fees under 37 C.F.R. § 1.20; or
- E. Any additional miscellaneous fees under 37 C.F.R. § 1.21.

6. A duplicate copy of this letter is enclosed for that purpose.

Respectfully submitted,

Dated: 10/26/01

By: Howard I. Grossman  
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TYPE OF DOCUMENT Patent Application

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Silicon interposer-based  
hybrid voltage regulator  
system for VLSI devices